# Mitchell On Demand 5.8.2.35 ((HOT)) Keygen Download

Oct 15, 2011 Mitchell OnDemand 5.8.2.35 Repair, Estimator, Manager Plus - Full Complect 2015Y 1st half EN Win (32/64-bit) iSO ~167 GB. May 26, 2012 I got a news that the new version is about to be released Mitchell OnDemand 5.8.2.35 Repair - Full Complect iSO (47 MB)" References Category:Installation software Category:Windows software Category:Automotive software1. Field of the Invention The present invention relates to a non-volatile memory device and more particularly to a NAND flash memory device that is electrically erasable and programmable and has a high integration degree. 2. Description of the Related Art In recent years, the integration degree of non-volatile memory devices has been increased in accordance with a requirement for large capacities of non-volatile memory devices. Examples of such non-volatile memory devices having the largest integration degree in practical use include a NAND flash memory device. A structure and an operation of a NAND flash memory device will be described with reference to FIG. 1 and FIG. 2. FIG. 1 is a plan view showing a memory cell array of a memory cell in a NAND flash memory device. FIG. 2 is a sectional view taken along line I—I in FIG. 1. In FIG. 1, a control gate transistor group is a group of N-channel transistors. Data lines, word lines, and source lines are arranged by a memory block, each having 32 to 64 memory cells. The control gate transistor group includes a plurality of word lines WL0 to WLn. The data lines D0 to Dn are arranged at an interval of eight memory cells. A memory cell M of the NAND flash memory device has a floating gate FG and a control gate CG. A source and a drain of the memory cell M are connected to the source line SL and the data line Dn, respectively. Also, the control gate CG is connected to one of the word lines WL0 to WLn. Each of the floating gate FGs of the memory cells M of a memory block is connected to the corresponding data line Dn. Thus, one memory block corresponds to one data line Dn. Each of the control gate CGs of the memory cells M of the control gate transistor group is connected to a common control gate line

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